WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

unit cells each including a cell transistor and a ferroelectric capacitor connected between a source and a drain of the cell transistor;

memory cell blocks each including the unit cells connected in series between a first terminal and a second terminal and a block select transistor connected between the second terminal and a third terminal;

bit lines each of which connects commonly the third terminals of the memory cell blocks;

word lines each of which connects commonly gates of cell transistors in the memory cell blocks;

block select signal lines each of which connects commonly gates of block select transistors in the memory cell blocks;

plate lines each of which connects commonly the first terminals of the memory cell blocks; and

a plate line driver to which a plurality of the plate lines are connected and which applies a potential to the plate lines.

2. The device according to claim 1, wherein the plate line driver includes first and second driver circuits, and

the memory cell blocks connected to each of the plate lines connected to the first and second driver

circuits respectively are connected to different word lines and different block select signal lines.

3. The device according to claim 1, wherein the bit lines include first and second bit line groups,

the word lines include first and second word line groups,

the block select signal lines include first and second block select signal line groups,

the device further comprises:

first and second column decoders which select any of the bit lines from the first and second bit line groups, respectively;

first row decoder which selects any of the word lines and any of the block select signal lines from the first word line group and first block select signal line group, respectively; and

second row decoder which selects any of the word lines and any of the block select signal lines from the second word line group and second block select signal line group, respectively,

the second column decoder and the second row decoder are inoperative when the first column decoder and the first row decoders are operative, and the first column decoder and the first row decoder are inoperative when the second column decoder and the second row decoder are operative,

the plate line driver includes first and second

driver circuits,

the memory cell blocks connected to the plate lines connected to the first driver circuit are selected by the first column decoder and the first row decoder, and

the memory cell blocks connected to the plate lines connected to the second driver circuit are selected by the second column decoder and the second row decoder.

4. A semiconductor integrated circuit device comprising:

unit cells each including a cell transistor and a ferroelectric capacitor connected between a source and a drain of the cell transistor;

memory cell blocks each including the unit cells connected in series between a first terminal and a second terminal and a block select transistor connected between the second terminal and a third terminal;

a first memory cell array in which the memory cell blocks are arranged in matrix;

first word lines each of which connects commonly gates of cell transistors in the same row in the first memory cell array;

first block select signal lines each of which connects commonly gates of block select transistors in the same row in the first memory cell array;

first bit lines each of which connects commonly

the third terminals of memory cell blocks in the same column in the first memory cell array;

first plate lines each of which connects commonly the first terminals of at least one of memory cell blocks in at least one row in the first memory cell array;

a first row decoder which selects the first word line and the first block select signal line;

a first column decoder which selects the first bit line; and

a plate line driver to which a plurality of the first plate lines are electrically connected and which applies a potential to the first plate lines.

5. The device according to claim 4, further comprising:

a first common plate line which connects commonly the first plate lines,

wherein the plate line driver applies the potential to the first plate lines via the first common plate line.

6. The device according to claim 5, further comprising:

element regions formed in a first direction and each shaped like a stripe extending along a second direction perpendicular to the first direction,

wherein:

the first word line extends over the element

regions and is shaped like a stripe extending along the first direction;

the first block select signal line extends over the element regions, and is formed adjacent to the first word line in the second direction and shaped like a stripe extending along the first direction;

the first bit line is shaped like a stripe extending along the second direction;

the first plate line extends over the element regions, and is formed opposite to the first block select signal line with the first word line interposed therebetween and shaped like a stripe extending along the first direction; and

at least part of the first common plate line is connected to one end of the first plate line and formed in the second direction at an end portion of the first memory cell array, and the first common plate line is connected to the plate line driver.

7. The device according to claim 4, wherein only memory cell blocks connected to any one of the first plate lines are selected in read mode.

8. The device according to claim 4, further comprising:

a second memory cell array in which the memory cell blocks are arranged in matrix;

second word lines electrically separated from the first word line and each of which connects commonly

gates of cell transistors in the same row in the second memory cell array;

second block select signal lines electrically separated from the first block select signal line and each of which connects commonly gates of block select transistors in the same row in the second memory cell array;

second bit lines electrically separated from the first bit line and each of which connects commonly the third terminals of memory cell blocks in one column in the second memory cell array;

second plate lines each of which connects commonly the first terminals of at least one of memory cell blocks in at least one row in the second memory cell array;

a second row decoder which selects the second word line and the second block select signal line in the second memory cell array; and

a second column decoder which selects the second bit line in the second memory cell array,

wherein the plate line driver is electrically connected to the first and second plate lines to apply a potential to the first and second plate lines.

9. The device according to claim 8, wherein the plate line driver is electrically connected to a plurality of second plate lines to apply a potential to the second plate lines.

10. The device according to claim 9, further comprising:

a second common plate line which connects commonly the second plate lines,

wherein the plate line driver applies the potential to the second plate lines via the second common plate line.

11. The device according to claim 10, further comprising:

first element regions formed in a first region in a semiconductor substrate in a first direction;

second element regions formed in a second region in the semiconductor substrate in the first direction, the first and second element regions being each shaped like a stripe extending along a second direction perpendicular to the first direction,

wherein:

the first and second word lines extends over the first and second element regions and each is shaped like a stripe extending along the first direction;

the first block select signal line extends over the first element regions, and is formed adjacent to the first word line in the second direction and shaped like a stripe extending along the first direction;

the second block select signal line extends over the second element regions, and is formed adjacent to the second word line in the second direction and shaped

like a stripe extending along the first direction;

the first and second bit lines are formed on the first and second regions, respectively and each shaped like a stripe extending along the second direction;

the first plate line extends over the first element regions, and is formed opposite to the first block select signal line with the first word line interposed therebetween and shaped like a stripe extending along the first direction;

the second plate line extends over the second element regions, and is formed opposite to the second block select signal line with the second word line interposed therebetween and shaped like a stripe extending along the first direction;

at least part of the first common plate line is connected to one end of the first plate line and formed in the second direction at an end portion of the first region;

at least part of the second common plate line is connected to one end of the second plate line and formed in the second direction at an end portion of the second region; and

the first and second common plate lines are connected to the plate line driver in a boundary region between the first and second regions.

12. The device according to claim 9, wherein only memory cell blocks connected to any one of the second

plate lines are selected in read mode.

13. The device according to claim 8, wherein only memory cell blocks included in one of the first and second memory cell arrays are selected in read mode.